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EMC
Product Design Guide

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EMC COMPLIANCE BY DESIGN

EMC compliance can be approached in several ways. The most common approach taken is to design the product for functionality and price and then to test the product to obtain final product certification prior to the marketing of the product. This approach is still the most common used and often results in band-aid and add-on fixes at the production stage to resolve emissions and immunity problems not taken into account in the initial product procurement specifications. In the majority of situations, a product stands ready to ship pending the final acquisition of the product certifications. The time spent in bringing a product into compliance after it has been designed and prototyped usually impacts the whole sales and marketing process and in some special cases, has been known to put a company under. Our most often made request when this happens is:

"Bring the product into compliance without making any changes!!!"

Sadly enough, we live in the real world of cause and effect and once the product has been finalized for production, the noise suppression options available to us reduces substantially and even these can be quite costly to implement in mass production runs. Statistically speaking, about 80% of the products we test for compliance need some degree of added suppression for emissions and/or immunity.

Since the subject of noise suppression is not taught formally in most universities and colleges, most design engineers will have to go through the school of "**hard knocks**" to acquire the experience and training in order to produce regulatory compliant designs. The design team can only do this through a coordinated effort involving both the mechanical and electrical departments since noise suppression is often three dimensional in nature. The best approach to compliance design is to be able to anticipate at each design stage, potential noise issues and to suppress them early in the design cycle. This is by far the best and most cost-effective approach and is one we highly recommend. Noise suppression in this way, can be taken one step at a time rather than waiting until the product is ready for production. Once this strategy has been adopted, the noise mitigation techniques will often be simple and straightforward to implement because there are less constraints on the techniques available.

Over design is part of an engineering trait used to provide a safety margin to take into account deviations of tolerances in components and processes. Bulletproofing a design from the viewpoint of noise suppression can only enhance the performance of the product especially in processing analog signals such as audio and video signals. Experience has shown that designs, which incorporate suppression at each design stage, have a 90% chance of meeting the final requirements without the need of additional suppression with the added benefit of improved signal integrity.

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THE COST OF NON-COMPLIANCE

The average cost of compliance increases on an exponential curve with respect to product development cycle. If taken into account in the early stages of product development, the costs are minimal. If left to the production or field retrofit stage, the costs can be exponential in nature and extremely prohibitive to implement.

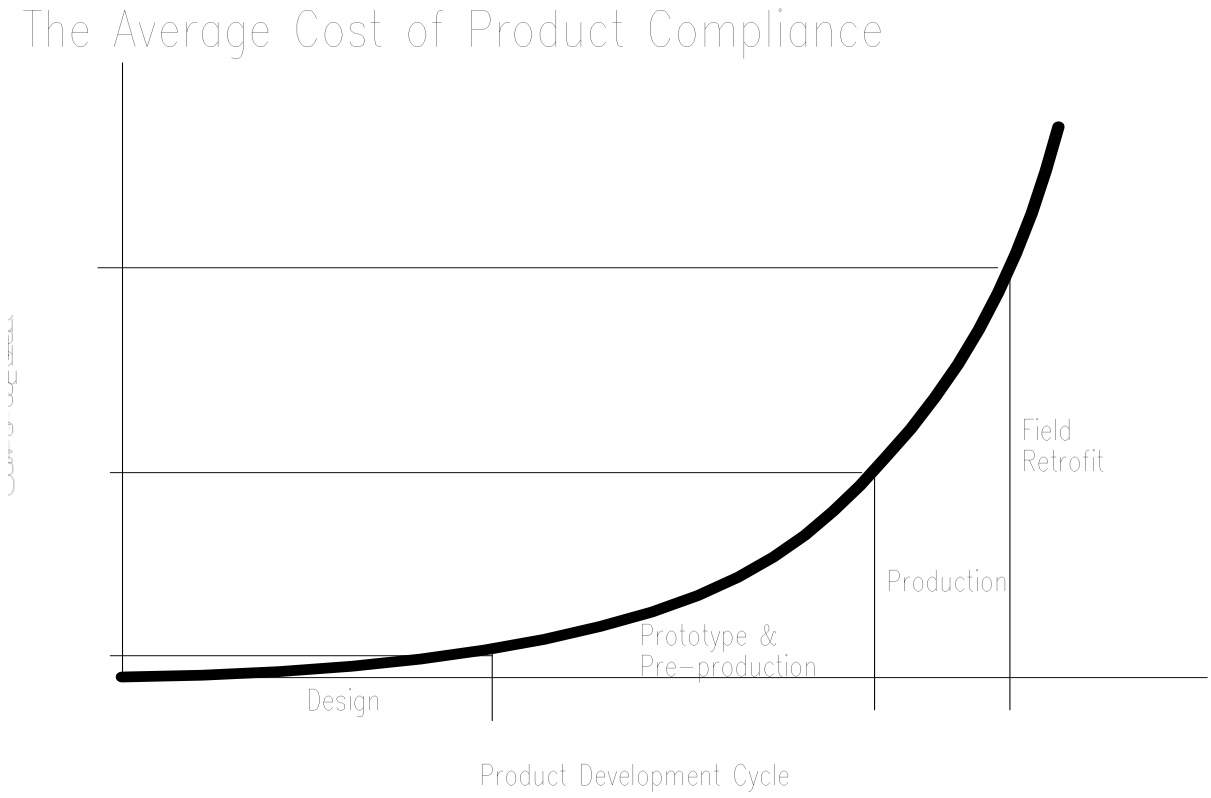

Figure 1 Exponential cost of mitigation

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THE PCB (PRINTED CIRCUIT BOARD)

The PCB is the primary originator of noise. As such the layout and structure of the PCB should be treated with paramount importance to noise suppression. It has been shown that the major contributing source to noise occurring on PCB structures is the common mode noise component and not the differential mode component.

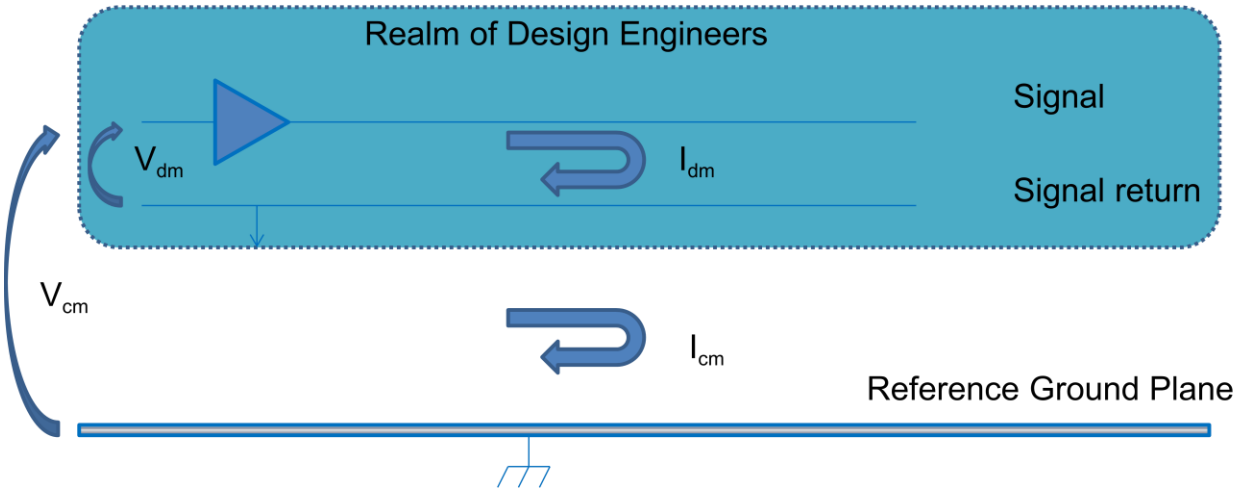

Figure 2 Common mode concepts

Single or Multilayer

The first step in PCB suppression is deciding on the PCB structure itself. i.e. single layer double sided, over a multi-layered board with embedded ground and power supply planes. EMC test engineers will tell you that multi-layered boards are quieter than equivalently laid out single layered boards. The degree of suppression offered by using a multi-layered board varies from anywhere from 8 to 15dB depending on the density of the board. The major drawback of going multilayer is the cost, which is usually more than double that of a single layered board. Obviously there is a trade off between cost and noise reduction. The choice of how many layers to use has often depended on the density and complexity of the circuit. Seldom has the high frequency content of a circuit entered into the decision of choosing the type of PCB to use. Even a simple circuit, which possesses many oscillator components, warrants consideration for going with a multi-layer design. This is not to say that a single layered board will not comply with the emissions or immunity requirements. Careful attention to layout and parts placement will often aid a design in meeting all the emissions and immunity requirements.

Choosing the right logic family

The basic rule of thumb is use the lowest speed logic family that your application requires - especially in critical areas such as buffers and drivers on data and memory buses. The fast rise times of high speed logic give rise to large overshoots and ringing which translate into high frequency content in the ensuing spectra.

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The characteristics of the most common logic families are provided as follows:

Logic Family	Frequency Limit (MHz)	Typical Rise-time (ns)	Typical Fall-time (ns)	Typical Slew rate (V/ns)
74	25	10.6	4.36	0.68
74LS	33	8.67	4.45	0.67
74ALS	35	7.27	7.27	0.85
74HCT	50	3.29	3.29	1.15
74S	95	5.0	3.05	0.98
74AS	125	3.9	3.28	0.9
74F	125	4.0	3.01	1.0
74G	1125	0.8	0.8	
ECLinPS	1,200	0.6	0.3	0.85
GaAS	15,000	0.04	0.03	0.075

*above data taken on a 10MHz clock signal

The above selection should be kept in mind when trouble shooting emissions problems as moving to a slower speed logic family on a critical IC can buy as much as 5dB in terms of noise suppression. This is especially true of buffers and bus driver chips since bus sizes of 16, 24 and 32 bit are not uncommon and the wider the bus, the more critical will be the choice of logic family. Often moving to a slower driver chip can result in a significant improvement in overall emissions characteristics without having to re-spin a PCB layout.

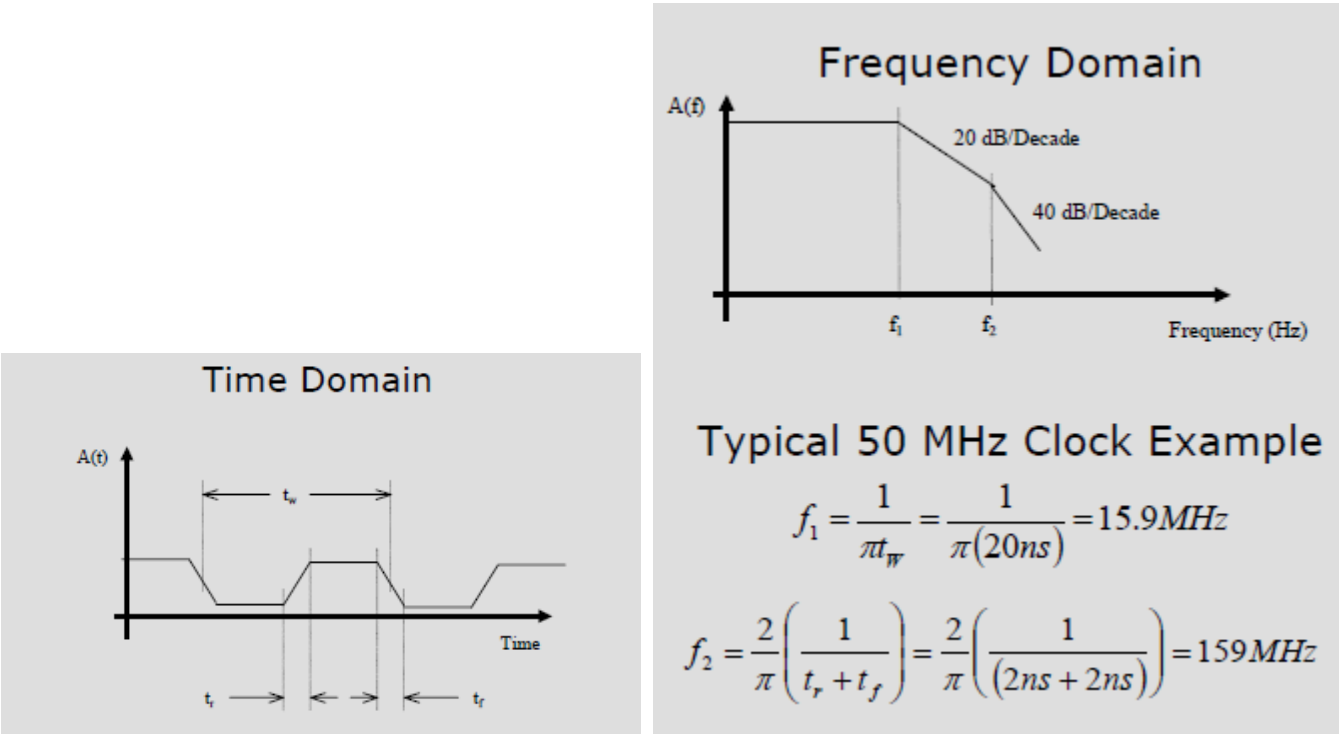

Figure 3 Slew rate spectral content

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The Current Loop

The most dominant mode of PCB radiation is the differential mode radiation arising from current loops arising when a current flows around loops formed by conductors in the circuit. The radiation (E) given off from these current loops are directly proportional to the area of the loop (A), the current flowing in the loop (i) and the square of the frequency (f).

$$E \propto Aif^2$$

Clearly to reduce E, the radiation from the loop, reduction of the area, current or the frequency in the loop must be carried out. Reduction of current loop is usually the easiest and most effective method. This usually involves placing the signal leads and their associated ground return paths as close together as possible. This is especially important for clock leads, back plane, bus runs and interconnecting cables. To get an idea of the largest allowable loop area, use the following formula:

$$LoopArea = \frac{380Er}{f^2 i} cm^2$$

where E: Limit in μV/m r: test distance in meters
f: frequency in MHz I: loop current in mA

Reducing Current Loops

Reduction of current loops can also be effected by the proliferous use of de-coupling capacitors between the power supply and signal ground pins of each IC. In single sided boards, de-coupling capacitors are more critical since the supply and ground traces are much longer and further removed from each other than in the multilayer case. Reduction of loop areas in this case is usually carried out using power supply and ground grids where power is run vertically on one side and ground is run horizontally on the other with connections made at the intersecting points by de-coupling capacitors.

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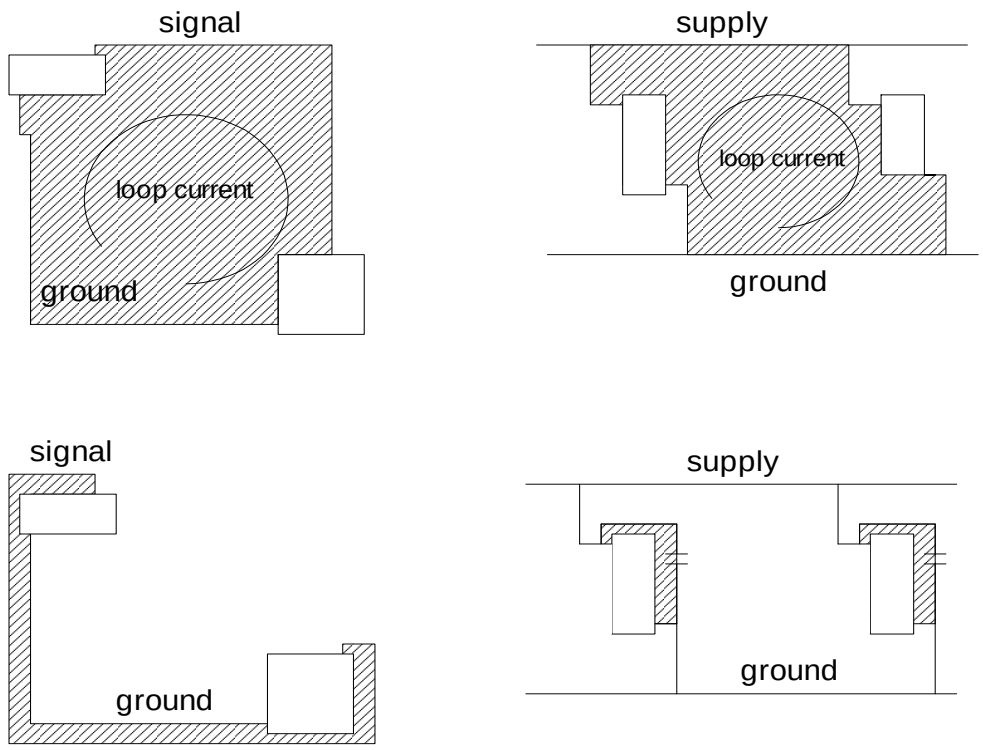

Figure 4 Current circumlocation reduction

Loop area reduction can be accomplished by the following procedures:

1. On all high frequency traces such as clock lines, ensure that there is a ground trace (guard trace) run along one or both sides of the trace or better yet, bury the trace between ground planes if it is a multi-layer layout. Enclosing the signal traces between the ground and power planes reduces both radiation and susceptibility to radiation. Keeping the trace length as short as possible will also reduce overall loop area.
2. On data and memory buses, ensure that there are ground traces run every two or three signal traces. This is obviously not required where a ground plane exists. This is especially important when the bus leaves the PCB using flat ribbon cable. Providing only one or two ground conductors on a flat ribbon cable is only asking for big, heavy, ugly flat ribbon ferrites to be added for additional suppression.
3. Provide de-coupling capacitors distributed throughout the PCB to tie the supply and ground grids together thus reducing loop area of supply currents.
4. Traces located near the edges of the PCB can radiate up to 20dB higher than when placed in the center of the PCB. Critical traces routed near the PCB edges should therefore be buried between ground and power planes to reduce edge radiation.

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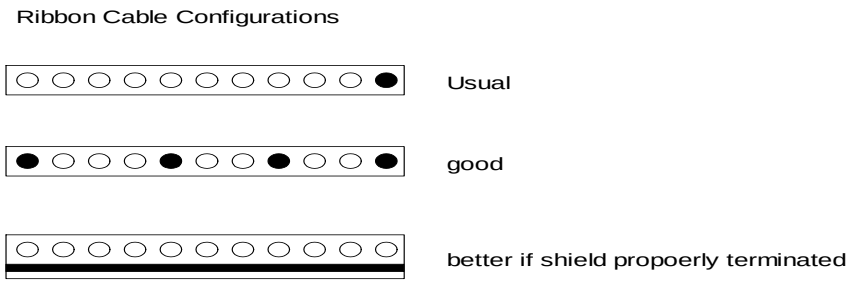

Figure 5 Bus and Ribbon cable return paths

Spread-spectrum clocking (SST CLK)

Spread-spectrum clocking is a recent technique that reduces the measured emissions using the standard EMI receiver, although it doesn't actually reduce the instantaneous emitted power so could still cause the same levels of interference with wide band responding devices such as radar and pulsed microwave systems. Spread spectrum modulates the clock frequency by 1 or 2% of the fundamental to spread the harmonics and give a lower peak measurement on commercial EMI receivers. The reduction in measured emissions relies upon the bandwidths and integration time constants of the test receivers, so is a bit of a trick, but has been accepted by the FCC and is in common use in the US and EU. The modulation rates in the audio band so as not to compromise clock square ness specifications. The following figure shows an example of an emission improvement for one clock harmonic.

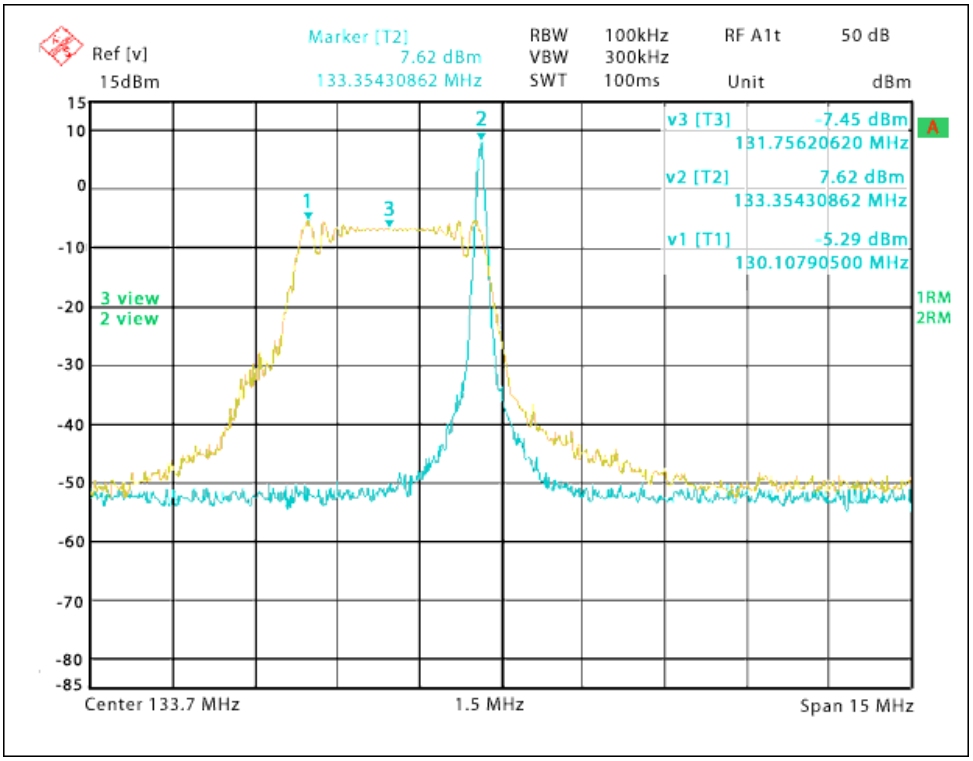

Figure 6 SST Clock emissions reduction

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Spread-spectrum clocking should not be used for timing-critical communications links, such as Fiber channel, FDDI, ATM, SONET, and ADSL.

Most of the problems with emissions from digital circuits are due to synchronous clocking. Asynchronous logic techniques will dramatically reduce the total amount of emissions and also achieve a true spread-spectrum instead of concentrating emissions at narrow clock harmonics.

The spread spectrum clock approach takes advantage of the noise measurement instrumentation used in determining the level of interference of a clock frequency's harmonics. It does not change the total power at each harmonic frequency, but rather disperses it out beyond the EMI receiver's 120kHz bandwidth so that it appears to the EMI receiver, that the peak level has dropped even though the total power has not changed. The higher the harmonic, the more the spreading effect. Although this is quite legal, it initiates debate over the validity of this technique to suppress or reduce the potential for interference since if the EMI receiver's bandwidth were wide enough to encompass the spread spectrum harmonics, there would be no level change in the reading due to the spreading function. Victim receivers with very wide receive bandwidths would therefore be at greater risk for interference from devices that have employed this technique o meet the regulatory requirements.

SST Clocks can now be found in all personal computer motherboards and are more recently showing up in Graphic processors and more surprisingly, Ethernet applications.

http://www.petermann-technik.com/fileadmin/pdf/PLL650-04.PDF

Calculation for SST dB reduction: Where; F = Frequency in MHz and BW = total % spread (2.5% = .025)

$$E_{SST_{dB}} \approx 6.5 + 9Log(f_{MHz}) + 9Log(BW_{\%Spread})$$

It is not uncommon for SST Clock to reduce emissions levels by 10-15dB and have often saved a PCB re-spin by installing a equivalent SST Oscillator package.

Power Grids

The use of power grids in reducing current loops is also effective in reducing the ground impedance formed by the inductance of the trace length. The longer the trace length, the higher the inductance. An interconnected grid will reduce the impedance considerably due to the parallel connection paths associated with the grid. Making the grid spacing as small as possible will thus reduce trace impedance as well as minimize current loop areas. Taken to the limit, this philosophy yields an interconnected ground and power plane, which is what multi-layered PCB's offer.

Avoid encircling the PCB with either the supply or ground trace as this will have the effect of creating a loop antenna that radiates rather than suppresses. A horseshoe configuration is better suited for this topology.

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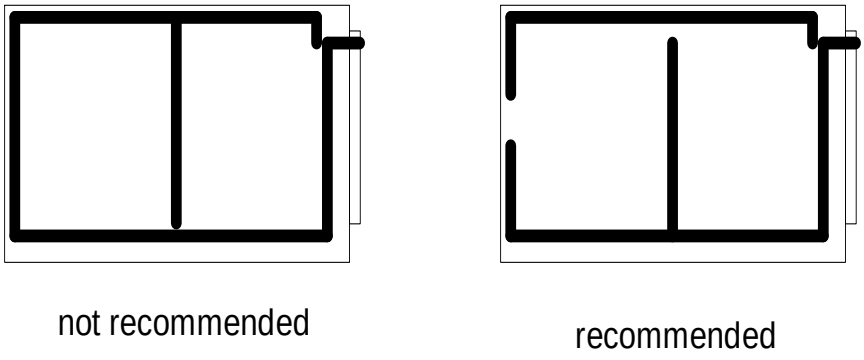


Figure 7 Prevent circulating currents

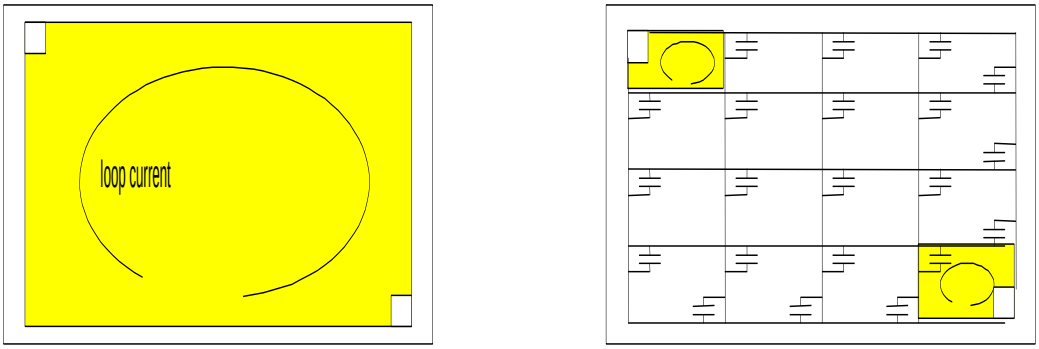
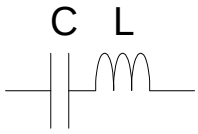


Figure 8 Breakup large circumlocation areas into smaller ones

De-coupling Capacitor Values

The size of the capacitor must be chosen carefully since the maximum effective frequency of a capacitor is limited by the inductance of the length of lead or traces connecting the capacitor to the de-coupling point. A circuit model of a real-life capacitor is:



$$f_{(res)} = \frac{1}{2\prod\sqrt{LC}}$$

At the resonant frequency of the capacitor f(res), the insertion loss is a maximum. The lead inductance can be estimated by the following formula.

$$L = 0.005Ln\left(\frac{4h}{d}\right)$$

d is the wire diameter in inches

h is height of conductor above ground

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The above equation assumes that h >> 1.5d.

Experience has shown that supply-decoupling capacitors in the range of 470pf-0.01uf are quite sufficient. For oscillator traces and clock leads, 47pf to 300pf are usually adequate depending on the drive capability of the source circuit as well as the frequency content on the trace.

To obtain a wider frequency response a high frequency capacitor may be paralleled with a low frequency one. Generally we use ceramic and mica capacitors at high frequency and tantalum capacitors at low. The axial mounted capacitors are preferable as they have lower internal inductance than radial components. Surface mount capacitors display the lowest inductance but the trace length still needs to be taken into account.

Capacitor Type selection

Type	**Maximum frequency**
aluminum electrolytic	100 kHz
tantalum electolytic	1 MHz
paper	5 MHz
mylar	10 MHz
polystyrene	500 MHz
mica	500 MHz
ceramic	> 1 GHz

Bulk de-coupling capacitors should be used where power enters the PCB. This capacitor should be at least 10 times the sum of the de-coupling capacitors on the PCB to provide an energy reservoir for charge storage to replenish the smaller de-coupling capacitors.

Matching the high speed clock lines

The primary cause of high frequency content in clock lines is the excessive ringing caused by impedance mismatch not taken into account during the PCB design cycle. This often arises when a driver with a high gate fan-out is used to drive only one or two gates. The result is often a mismatched transmission line with a high content of reflection occurring on the line causing much of the energy propagated along the line to be radiated off into free space. In order to reduce the reflection a matching resistor of 20 to 33 ohms may be placed in series with the line at the source end. It is important as to the placement of the matching resistor as a circuit schematic may depict it in the circuit but the PCB layout may place it less than close to the drive end of a line.

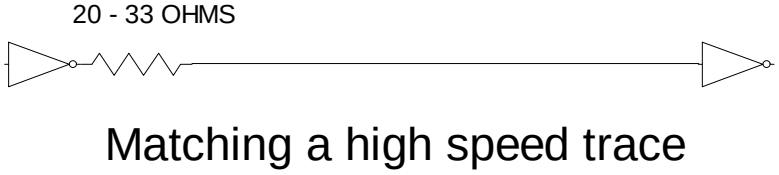

Figure 9 Transmission line impedance matching to reduce ringing

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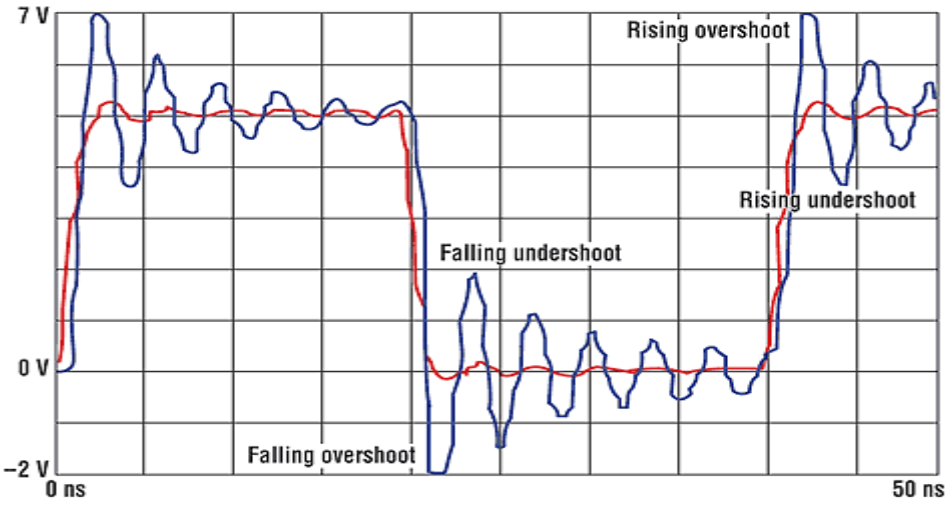
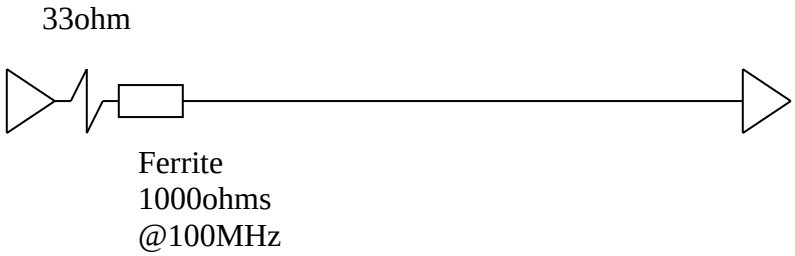


1. On nets with fast drivers, signal-integrity effects are often categorized as overshoot, undershoot, and ringing. Crosstalk also can produce the same effects, or affect timing to the point where the logic no longer operates.

On very critical clock feeds, a series ferrite may be added to further help shape the time domain waveform and limit the amount of high frequency harmonics traveling down the trace. It is important to locate the matching resistor and ferrite as close to the source end as possible.



Additionally, a capacitor may be added at the load end of the transmission line to control high frequency harmonics.

The strategy on clock lines is provide pads for suppression components in the event they are needed. This will save PCB re-spins when emission levels prove too high to suppress by non PCB remedies.

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Isolating PCB Areas

PCS layout should be grouped into the following areas for layout:

- High Speed Logic
- Medium Speed Logic
- Low Speed Logic
- Analogue
- Interface

Each area should be defined and isolated as much as possible using separate supply and ground grids, which are joined only where the power enters the PCB. Further circuit isolation may be achieved by the use of PCB fences to completely shield a noisy section of the PCB from other, more sensitive areas. This technique is commonly used in radio and TV circuits to prevent local oscillator signals from interfering with high fidelity audio and video circuits. If PCB fences are used then there must be additional care taken to band limit traces entering or leaving the enclosed area as these are potential paths for emissions to leak away from the isolated section. This is especially true if internal cables are interconnecting to the isolated section.

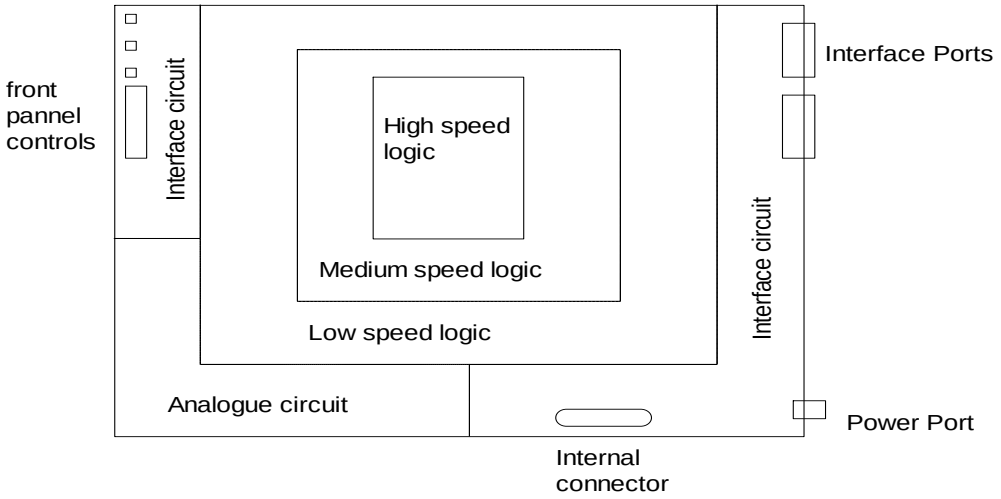

Figure 10 Isolating PCB zones by function

Further isolation may also be obtained by enclosing areas of high emissions with tin or mesh covers that are tied into the ground plane. Another technique used in the isolation of critical areas is the picket fence approach where vertical ground vias can provide the isolation along the PCB edges as well as between separate circuit regions by “stitching” the copper planes together at the edges.

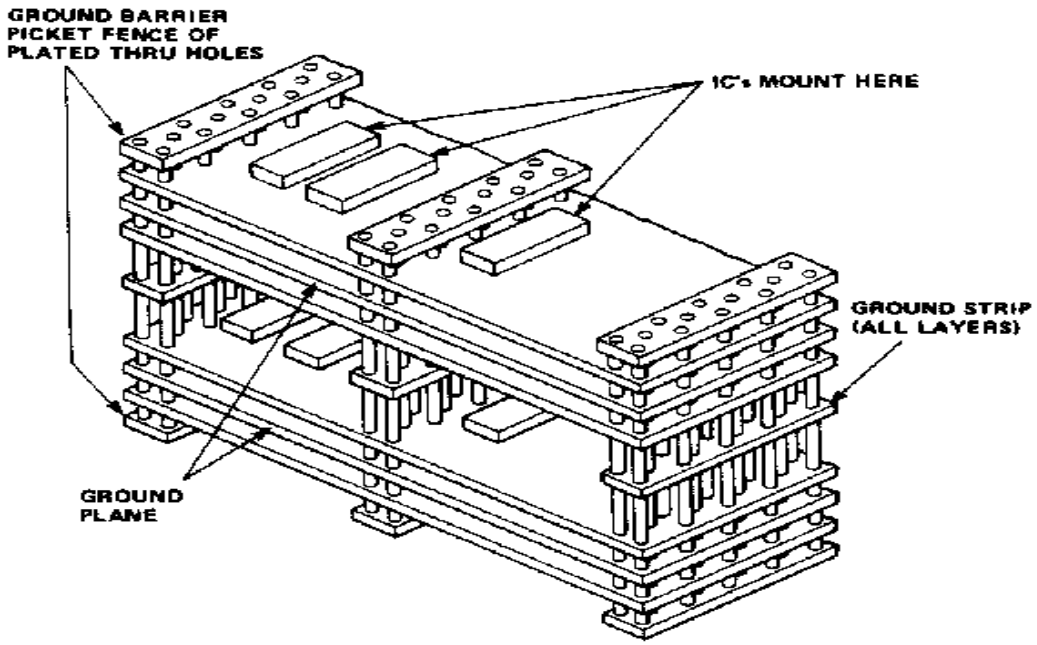

Figure 11 Picket fence using vias to demarcate PCB areas

Interface and Connector Ports

All intersystem interface and connector ports should have all leads (both signal, dc power, and grounds), band limited using de-coupling capacitors and/or ferrite chokes. If the lead is not band limited in some way, they pose a potential path for emissions to gain entry or exit to/from the PCB. Typical values for I/O de-coupling capacitors are 470pf to 2200pf to chassis ground. If shielded cables are used, care must be exercised to ground the shield of the I/O connector shell to chassis ground and not directly to the signal ground of the PCB. This may require some special requirements for bringing the chassis ground directly to the I/O interface area through metal mounting standoffs.

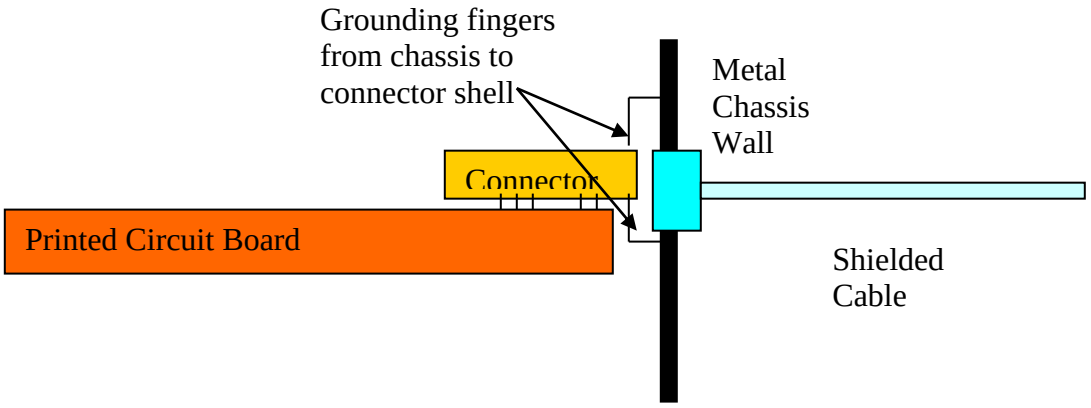

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Figure 12 Typical Shielded I/O Connectors mounted directly on PCB

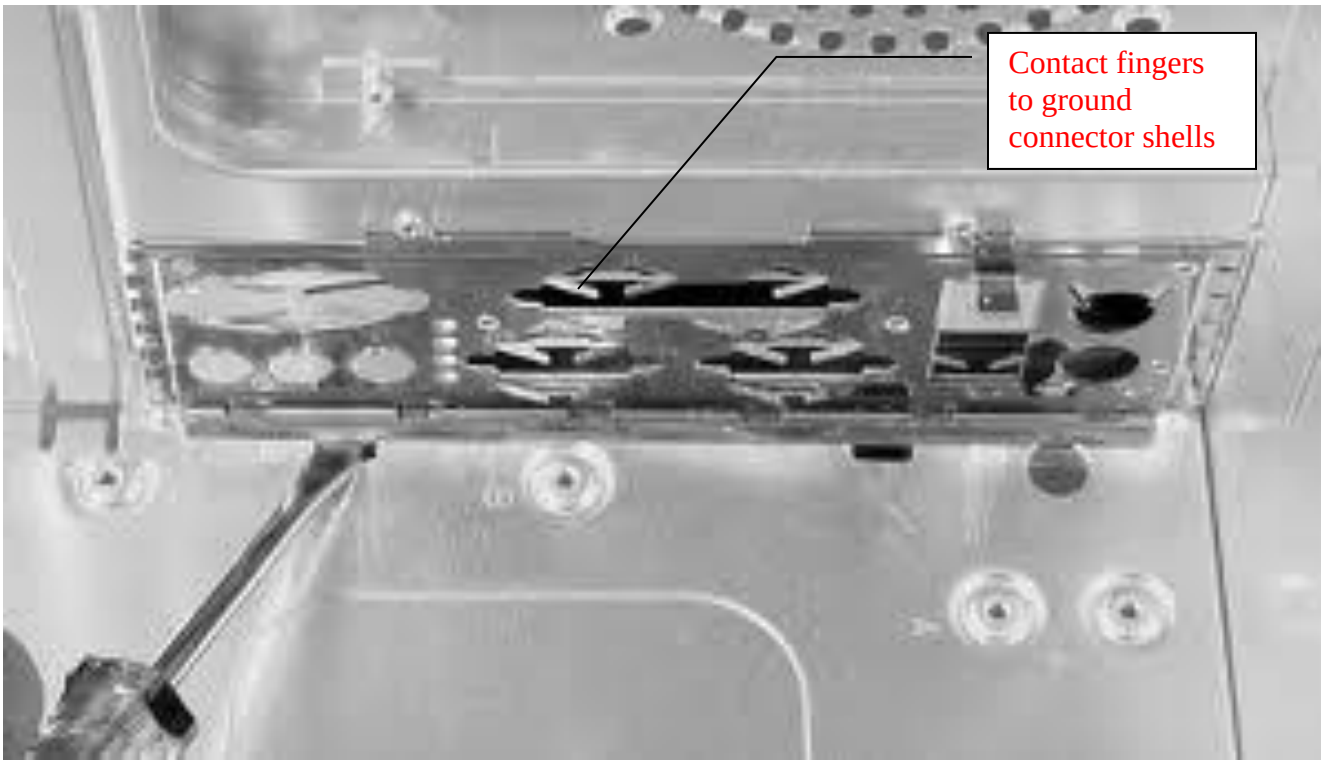

Figure 13 I/O Panel Interface providing chassis grounding tabs to shielded connector housings

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Component Placement and Layout on the PCB

Before beginning to layout a PCB, the first step is to identify all critical components that affect the emissions characteristics of the board. These would be:

- Crystal oscillators
- CPUs, video processors and I/O processors
- Clock division and driving circuits
- I/O circuitry
- Memory blocks

The next step is to locate the interconnecting components as close together to minimize trace run length. This usually means oscillators, processors and clock regeneration and divides down circuits in very close proximity. Placement of these high frequency elements is critical and is usually relegated to the center of the board away from all I/O connectors and internal cable runs and jumper straps. The memory chips should be laid out so that overall loop areas are minimized.

After the main component locations have been selected, concentrate next on the ground return paths for each of the high frequency signal traces. For multilayer boards this is usually not an issue but on double sided single layer boards, this step is of paramount importance. Each high-speed signal trace should have a ground return path run next to it or even on both sides of it.

Where buses are run along the board or to a back plane, it may not be possible to provide a ground return trace for each signal. The alternative is to provide a ground for every two or three traces. The effect here is to reduce the loop areas in the bus run. This is especially effective if the bus is extended off the board by dip header or ribbon cables.

Another must at this stage is to consider what-if scenarios in the event additional suppression is required in the finished product. After all, odds are that there is only a 20% chance that you won't need additional suppression. Provide pads or through-holes for the mounting of suppression components on all signals going to the I/O interfaces. The mounting points must be as close to the I/O connector as physically possible to reduce coupling back onto the I/O signals after the filters. Any unused signals on the I/O interface should be tied to ground directly or through a capacitor. For the oscillators and clock driving points, provide mounting points between clock output and ground for smoothing capacitors. If the clock traces are long and not buried between ground and supply planes, provide mounting points for ferrites and capacitors at one or two points in the trace run.

The oscillator cans usually provide voltage swings in excess of 7 volts; in most cases a 3-volt swing is sufficient. Reducing the voltage swing of clock signals by selecting low output oscillator modules will certainly help as will rounding the output of the oscillator using capacitors. This being the case, another way of reducing the voltage swing on the oscillator output is to reduce the supply voltage from 5 volts to say 3 volts using a voltage divider or resistor in the supply lead.

Mounting pads for resistors or ferrites can be placed along the trace run and if these become needed, the trace between the pads can be cut very easily. These suppression points may or may not be used depending on the

results of the pre-scans but if they are needed, the mounting points will prevent the need of re-laying out the PCB.

The PCB should start to fill up by now and power and ground traces for the other components should be run to determine de-coupling points throughout the board for the power grid formation. Make sure that for each IC there is a de-coupling capacitor between supply and ground. Remember, the smaller the grid the more effective the ground plane becomes in suppressing unwanted noise.

There are usually several mounting points on a PCB to prevent flexing of the board. Provide grounded pads on these mounting points throughout the PCB to connect signal ground with chassis ground. Should isolation at certain points be required, nylon standoffs or washers may be used.

If you have followed the guidelines above, the PCB should be much quieter than letting the auto-router do the work and the finished product will have a higher likelihood of meeting the emissions and immunity requirements. Unfortunately a well laid out PCB does not necessarily mean instant compliance since it is only one component in the system where component interaction plays an important part.

PCB Plane Topography and edge effects

Emissions from the edge of PCB's may be reduced by backing off all copper planes above and below the ground plane, a few millimeters from the PCB edge. This reduces the emissions leaving the edge of the PCB structure. This technique is often referred to as the `20h`rule where the offset is determined by 20 times the plane separation. http://www.montrosecompliance.com/upload/20-H_rule_paper.pdf

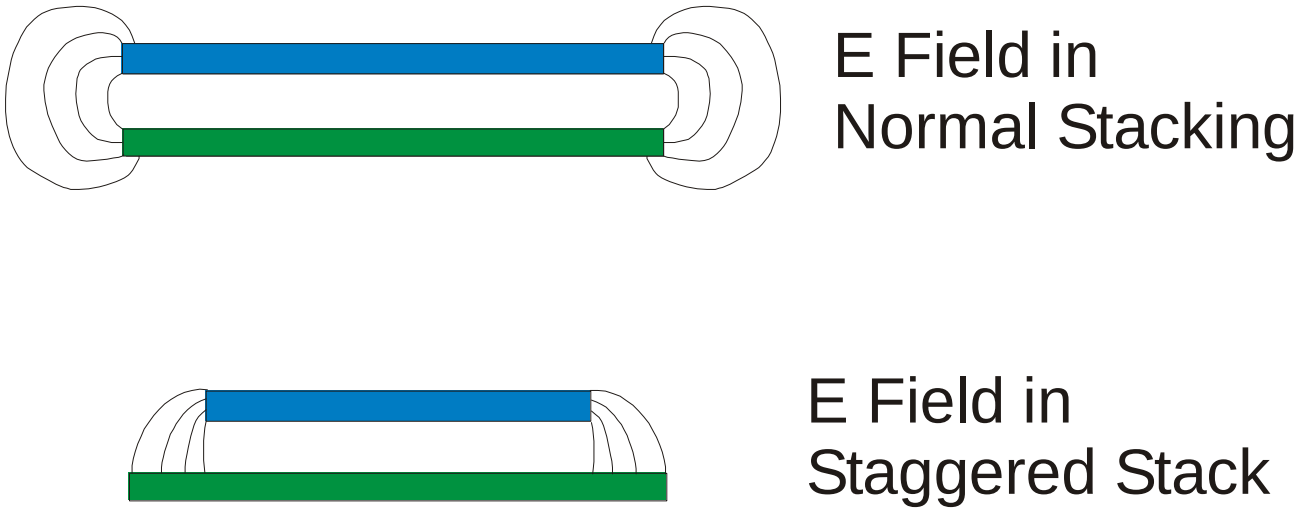

Figure 14 Extended Ground Plane reduced edge effects

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The PCB area under I/O Connectors

The most common practice in treating the area surrounding I/O connectors is that this area deserves no special treatment and that all copper planes are allowed to flow under I/O connectors. This is quite misguided as any copper introduced into the I/O connector area, will provide a coupling path for emissions quite often by-passing filters placed on the PCB structure to eliminate unwanted emissions from coupling onto the I/O connector and cables. The most common misconception is that the ground plane is quiet and therefore does not provide a coupling path for filter bypass to occur. As it turns out, the signal ground plane is usually the noisiest common mode source of emissions and is most likely the worst culprit of all the copper planes affecting I/O connector ports.

The rule of thumb here is to isolate I/O connectors so that only "clean" copper goes anywhere near the I/O connector or its attached cable and it is not only on the PCB that this rule must be applied. "Clean" copper is defined as traces that have been filtered of unwanted emissions using capacitors to chassis ground, ferrites or common mode chokes. If the PCB resides inside a metal chassis, then the chassis ground must be somehow introduced onto the I/O connector area at multiple points in this area. All filter components must be carefully located to minimize the introduction of noisy traces into this quiet area of the PCB.

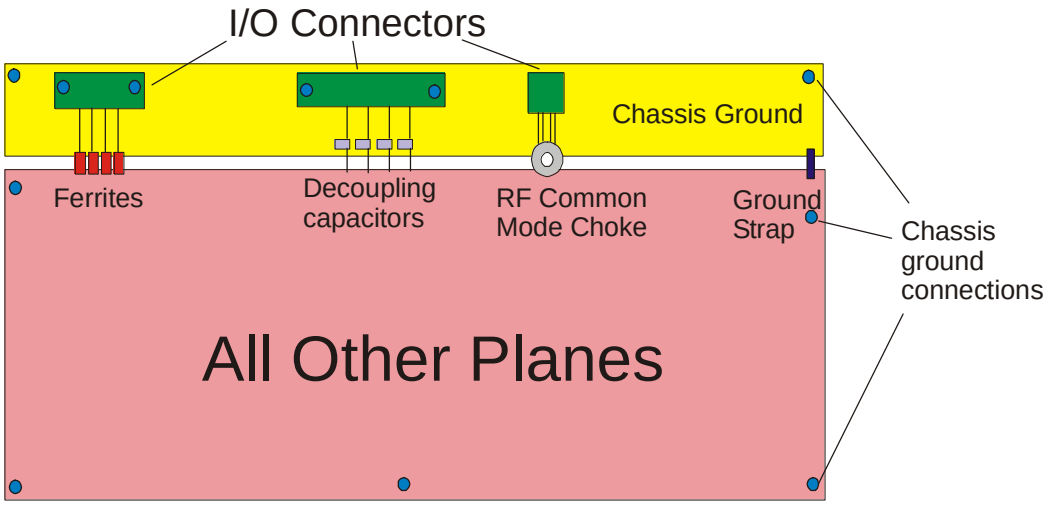

Figure 15 Introducing chassis ground onto PCB - keep it isolated

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Filter Bypass

Filter Bypass occurs when noise couples from the input to the output side of a filter due to other paths not considered in the circuit design. The Filter bypass will compromise the insertion loss of the filter element and in some cases may render the filter completely ineffectual in function. The most common filter bypass occurs in the multi-layers layout in a PCB. The most common practice on Multi-layer PCB's is to flood the PCB with Vcc and signal ground planes. The diagrams below depict filter bypath paths which can severely compromise filter elements on the PCB.

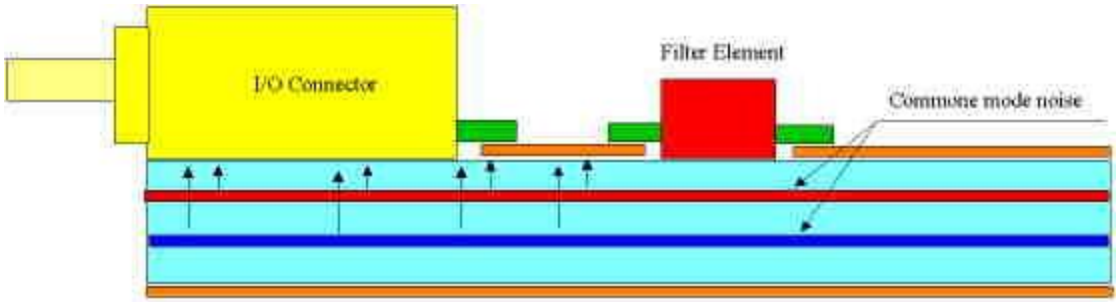

Figure 16 PCB Filter by pass

To ensure the filter elements are not being bypassed, care should be taken to ensure that copper planes are pulled back from the filtered area of the PCB. The only copper plane appearing under the filtered area should be Chassis ground introduced on the PCB for decoupling capacitor filters.

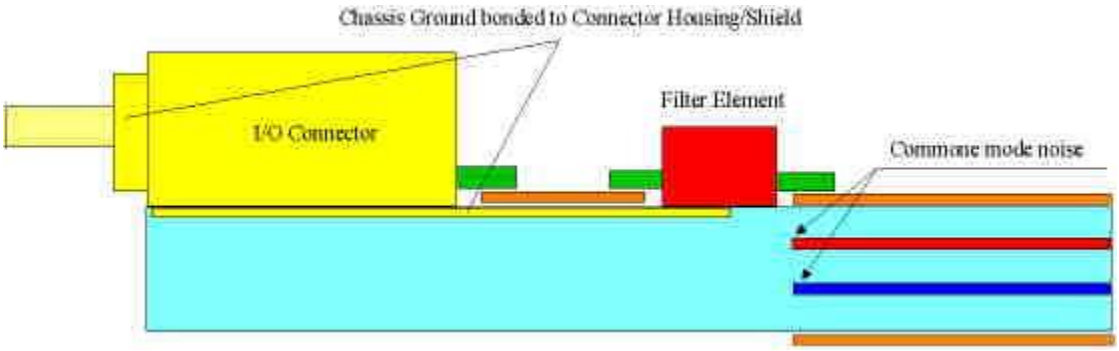

Figure 17 Isolation of connector/Filter area prevents filter bypass

In the event no decoupling capacitors are used and only common mode or discrete ferrite elements are used then the filtered area of the PCB should only contain the filtered traces leading to the I/O connectors.

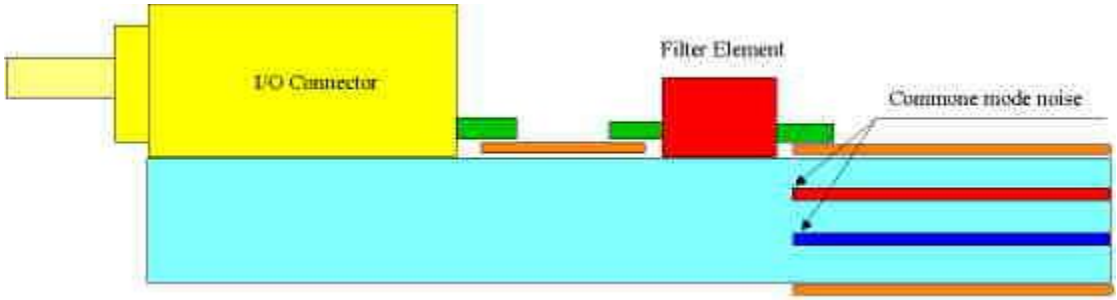

Figure 18 Only clean traces/copper allowed onto I/O connector islands

Operational amplifers, comparators and buffers

Operational amplifers are used widely in processing and amplifying analogue signals in PCB designs are in themselves are very susceptible to RF common mode noise at the inputs to the op-amps. The CMRR (common mode rejection ratio) specified for op-amps are restricted to their in-band performance and no data is provided for out-of-band CMRR. No-one knows how an op-amp will perform when subjected to a 50MHz common mode RF signal and design engineers should take this into account by providing common mode filter elements at the inputs of the individual op-amp stages. These may be a combination of common mode chokes, x/y ceramic capacitors or high impedance ferrite beads. The selection will be dependent on the type of signal the op-amp will be called upon to process.

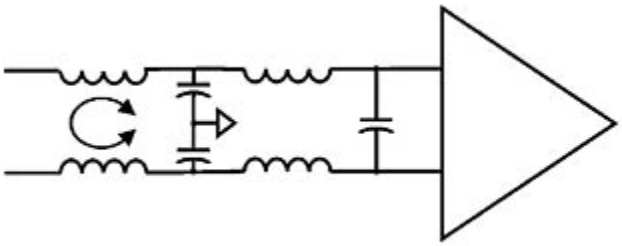

Figure 19 Common mode filters prtoect op-amps

It is important to select op amps (Operational amplifiers) with a high EMIRR (EMI rejection ratio) in mission critical circuits to alleviate to prevent un-desirable affects from common mode noise. More information on EMIRR can be found at the following links with the appropriate EMI hardened op-amps;

1. http://www.ti.com/lit/an/sboa128/sboa128.pdf
2. http://webench.national.com/assets/en/appnotes/national_AN-1874.pdf

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Hardening Reset lines

The reset circuits are often upset by transients such as ESD (electrostatic discharge) or EFT (electrical fast transient). A secondary threat is RFI (radio frequency interference.). It is important to ensure that the reset signals are not edge triggered but are level triggered and that the reset signal is not un-intentionally initiated.

Use of de-coupling capacitors or lower resistive pull-up/down devices are commonly used to harden these critical circuit areas. Other methods include implementing a validation protocol by averaging sampled signals in software before responding to a reset signal. All these methods may be used to effectively harden the system to inadvertent resets.

ESD Countermeasures

ESD effects account for a high amount of excitement relative to the other immunity tests performed. The ESD event is a 1.5GHz kilo-volt nanosecond event that really tests out the high frequency bonding of a products internal structure. If all metal components jump to the same potential during the ESD event, there will be no induced current between conductive components. However, if the interconnecting ground bonds between internal parts are not sufficiently low in impedance; significant potential differences between interconnected parts will cause high peak currents to flow through the grounds of the interconnected parts causing significant ESD threats.

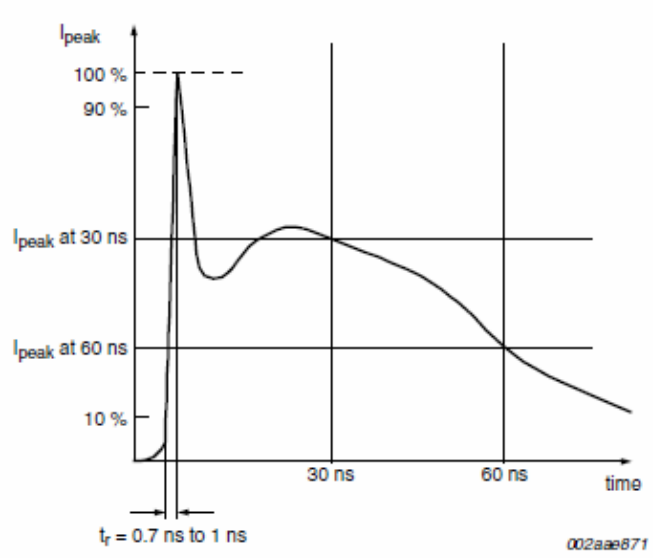

Figure 20 ESD Current Waveform

Effective ESD countermeasures are usually of two forms; Insulation or ESD current path re-routing (shunting ESD currents to Ground). Depending on the ESD threat, either method should be explored to determine optimal efficacy. Insulation may take the form of heat shrink tubing, rubber housings, lexan panels and plastic covers. Shunting ESD currents to ground may involve supplementing ac safety grounds with braid

straps, installing tranzorbs or protection diodes or applying protective grounded metal collars to sensitive touch areas.

Watch Dog Timers

Watch dog timers are an inherent part in improving the recovery of a product from any system upsets caused by EMC phenomena. These can be implemented both in hardware as well as in software where if the main processor is hung, a system level reset can be initiated to recover the functionality of the system. Watch dog timers are especially useful in USB applications where occasionally the USB connection is lost. Having some mechanism to detect this and re-initialize the USB driver can remedy this event.

Transient Protection

Transient protection is an important part of preventing upsets from fast transient and surge events entering a product through the power lines or the I/O ports. Transient protection can come in the way of various suppression devices such as diodes, varistors, thyristors, transzorbs, de-coupling capacitors, gas tube arrestors and PTC polyswitches. Each of these devices have their limitations and it is important to be aware of these as some application may prevent their use.

- Diodes - Diodes are commonly used in low voltage protection areas such as I/O ports and power supplies where reverse-biased zener diodes/Transzorbs are employed to limit the voltage excursions. These devices are small in nature and cannot absorb much energy before failing. A diode usually will fail short so a current limiting device is usually used in conjunction to prevent fire-hazards from occurring on the PCB depending on the current potentials involved.
- MOV (Metal Oxide Varistors – MOV's are slower than diodes in response and do not respond to fast transients but are really designed for the slower exponential surge voltages that pack more energy. As such, they can absorb more energy during the surge event but they are much larger disc type devices that have a tendency of also failing short. Because of this, the safety agencies are very cautious of their use and often require current limiting elements on both line and neutral in front of the MOV's to prevent fire-hazards on the PCB.
- Gas Tube Arrestors – These devices are based on the spark gap principle where a certain voltage protential will trigger a spark across a designated gap. Once the spark is initiated, it will not quench until the voltage across the gap reduces to zero. Spark gaps fail open so do not have the same safety consequences as MOV or Diodes.
- Current limiting devices – Fuses, resistors, PTC polyswitch are all current limiting devices used to protect devices from high input surge currents. Fuses are the most common devices but suffer from their single use protection mode and can lead to nuisance field failures costing high maintenance penalties on an installed product base. Flame proof resistors are a more robust way of limiting current but the degrade the energy efficiency of a product. PTC polyswitches have become a more viable way of dealing with limiting current during surge events as these devices will open quickly and eventually reset once the device is allowed to cool down.

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THE POWER SUPPLY

Most power supplies are Switch Mode because they are more efficient, lighter, smaller, and cheaper and they have the ability of accepting a wide voltage range for international operation. Their major drawback is that they are noisy if not designed with care, and can often lead to product failure due to conducted and radiated emissions. Most system designers prefer to purchase open fame supplies that have all the safety approvals already performed. The main advantage of this is that the product manager has one less headache when it comes to gaining the regulatory approvals

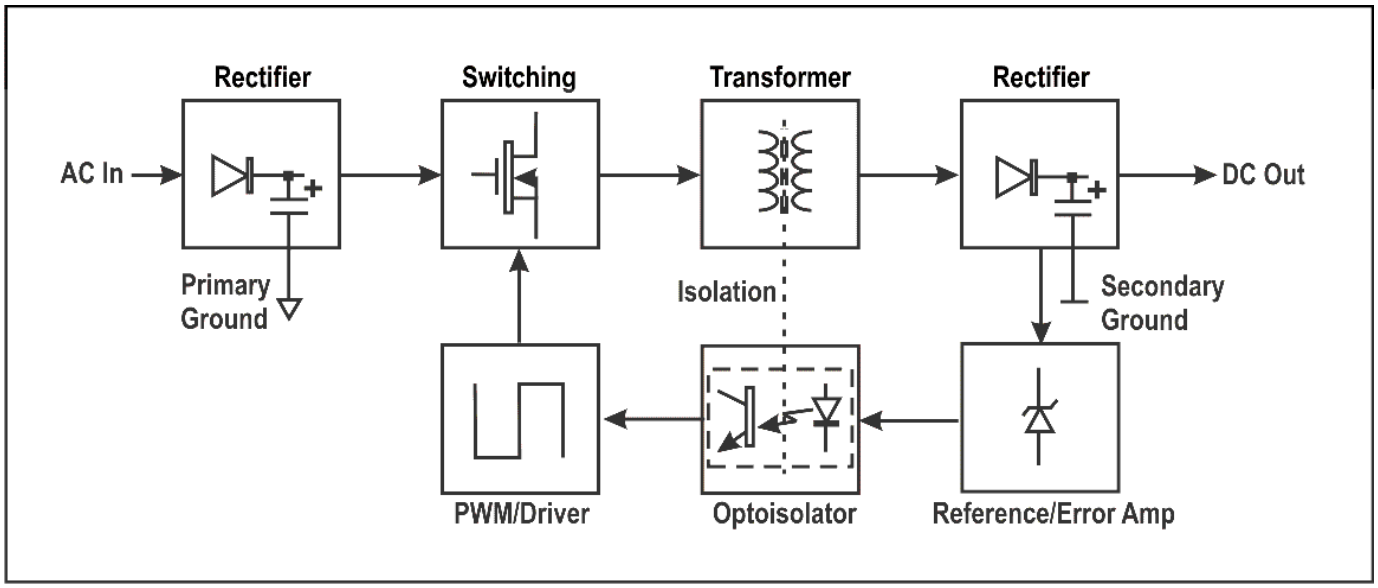


Figure 21 Switch mode power supply block diagram

Filtering of AC power line

In order to design an effective power line filter, the frequency and type of noise must first be determined. Two types of conducted emissions modes exist, the differential component and the common mode component. Comparing spectral conducted emissions plots of the spectrum can determining which is the dominant component (http://www.hottconsultants.com/techtips/CM_vs_DM%20Conducted_Emission.html). If the emissions are very similar in nature as is generally the case for symmetrically designed EUT power supplies, then the dominant component will be the common mode noise between phase to ground and neutral to ground.

Placing capacitors between phase and ground and neutral and ground can effect filtering of the common mode component. The larger the capacitor, the more effective will be the filtering. In addition, as the capacitor value increases, so will the leakage current and a trade off exists between meeting safety standards and meeting EMI conducted emissions limits. Should the capacitors prove insufficient in attenuating the conducted emissions below the limits, common mode chokes in line with the phase and neutral may be added to provide additional insertion loss. Commercial power line filters are available for this purpose and can provide insertion losses of 40 to 80 dB.

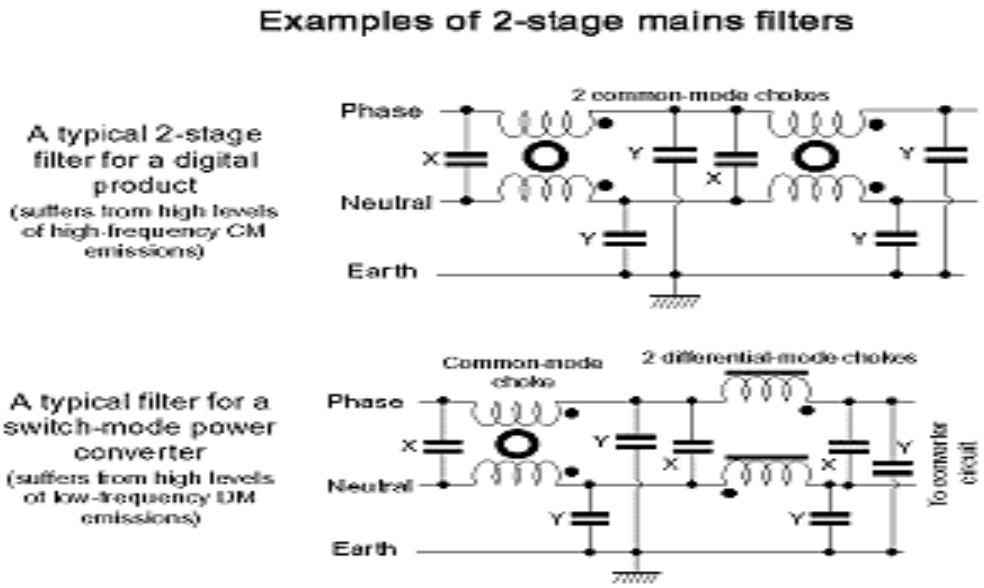
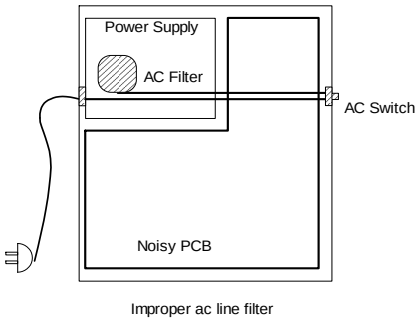
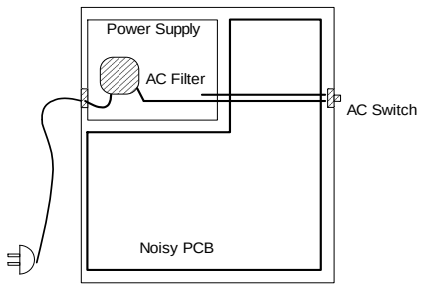


Figure 22 AC common filters

The location of the power line filters is as important as the filter components themselves. Ideally the filter should be placed at the entrance of the power cord to the chassis. Improper placement will defeat the purpose of the filter and allow noise to couple back onto the cable behind the filter. The best AC line filters are those with the filter incorporated within the connector housing. These types of filter prevent incorrect placement and are highly effective in reducing the emissions on the ac lines.



Improper ac line filter



Proper ac line filter

Figure 23 AC Filter location is critical to its performance

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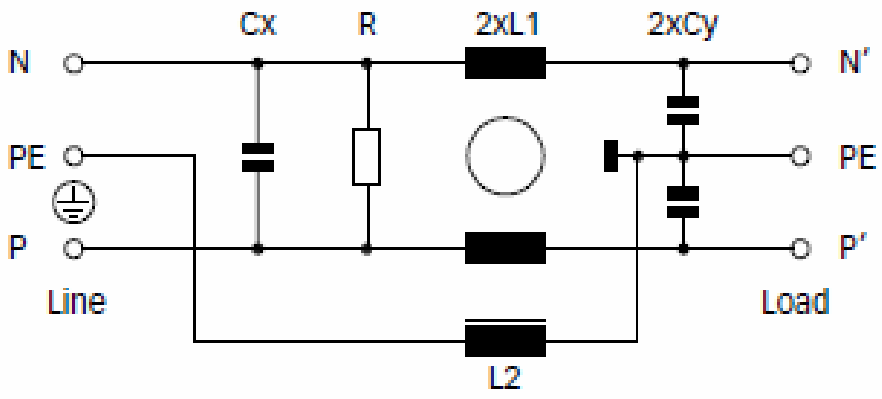
Suppressing ground loops

Occasionally, the earth ground of the ac line becomes contaminated with ground loop currents and this can be suppressed using additional RF chokes in the earth ground. There are specially designed AC line inlet filters that address these types of situation as well as individual earth ground chokes designed to meet the ground bond tests.



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Switch Mode Device Transients

The MOSFET is most often used to drive the high currents needed in s SMPS circuit and as such is the source of many of the harmonics generated in the SMPS circuit. Suppressing the harmonic rich ringing of the current switch will go a long way in EMI mitigation. There are two methods of accomplishing this and the more common approach is to add a snubber circuit in the source of the FET. Another technique we have found effective especially in the above 30MHz spectrum is to limit the gate drive current using resistors or ferrite beads. Since the gate current is often very low, ferrite beads will not saturate and will limit the high frequency content driving the MOSFET.

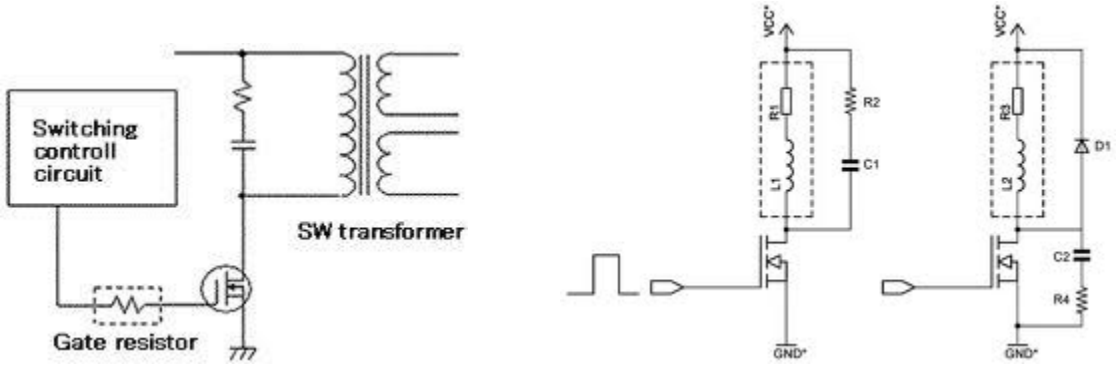

Figure 24 Limiting gate drive current and snubbing the source on MOSFET

Transformer concerns

Common mode currents can traverse a transformers isolation through parasitic capacitance between the windings. This can be alleviated by application of y-capacitors between the primary and secondary returns of the transformers. (Note. It is critical to place this y-cap at the transformer terminals and not at some far location on the PCB for this to be effective).

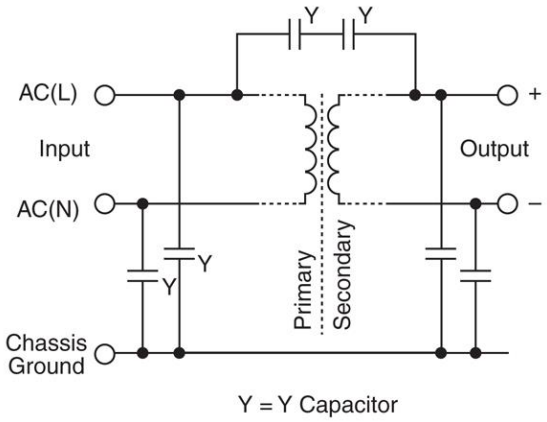

Figure 25 Y-capaictance provides a path back from common mode currents coupled across windings

An alternate method of alleviating common-mode currents from traversing the windings of a transformer is to employ shielded transformers with electrostatic shields between the windings.

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Snubbers on Output Diodes

Output diodes that drive the rails of an SMPS circuit are often overlooked as being the source of EMI but they do contribute a significant portion to emissions on the DC side of the SMPS. (Just because its DC does not mean those lines don't radiate!). It is often wise to put in the pads for RC snubber networks on all output diode drivers. Initial values we recommend are 10ohm/1000pf but these can be adjusted in practice.

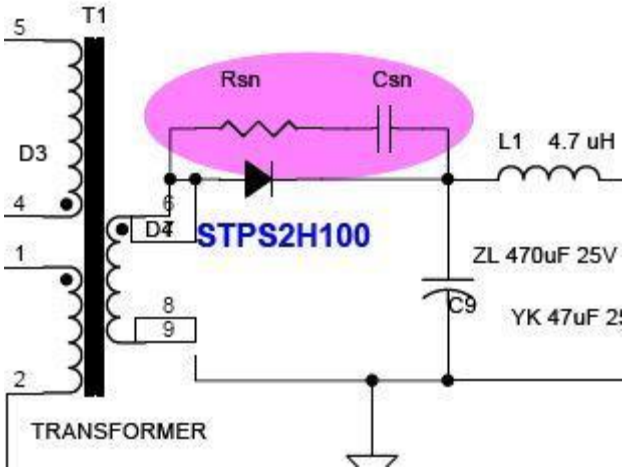

Figure 26 RC Snubber on Output Diodes

An alternative to employing snubbers on the output shottky diodes is to use a slower diode sometimes referred to as stealth diodes. These diodes exhibit low reverse recovery current and very soft recovery thereby minimizing the ringing associated with the faster shottky type diodes. A good article on various diodes for SMPS applications is;

http://www.powerguru.org/2012/08/10/the-application-specific-power-semiconductors-diodes/.

DC output Common-mode Filter

The dc output rails are often overlooked as sources for common-mode radiation since it is believed that DC lines do not contain high frequency components as it is heavily filtered using high value electrolytic capacitance to signal ground. In practice, we see more issues associated with common-noise emitting from the DC output side of SMPS since it is widely accepted that the AC line must be properly filtered to meet conducted AC emissions requirements. The most cost effective way of reducing the common mode emitting from the DC output lines is the use ceramic de-coupling capacitors to chassis ground on all the DC rails and returns. Additional suppression can be obtained using common-mode chokes on the DC output lines which includes the signal return lines. This is not as straightforward as it seems since the rails will have different current capabilities and the DC currents may saturate the ferrite material thereby compromising the insertion loss provided by the choke.

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I/O CABLES AND CONNECTORS

Cables and associated connectors are a number one cause for non-compliance among computing devices. It is therefore important to tell what type of cables should be used when carrying out EMI qualification tests. A well-designed cable will maintain the shielding integrity of the two devices it is serving to interconnect. Think of a cable shield as an extrusion of the metal chassis it connects to.

An ideal connector uses a metallic housing that completely encloses the connector wiring and makes 360-degree contact with the cable shield and the mating connector that is bonded to the Chassis. Thumbscrews or locking nuts are also used to ensure a tight fit for good electrical bonding.

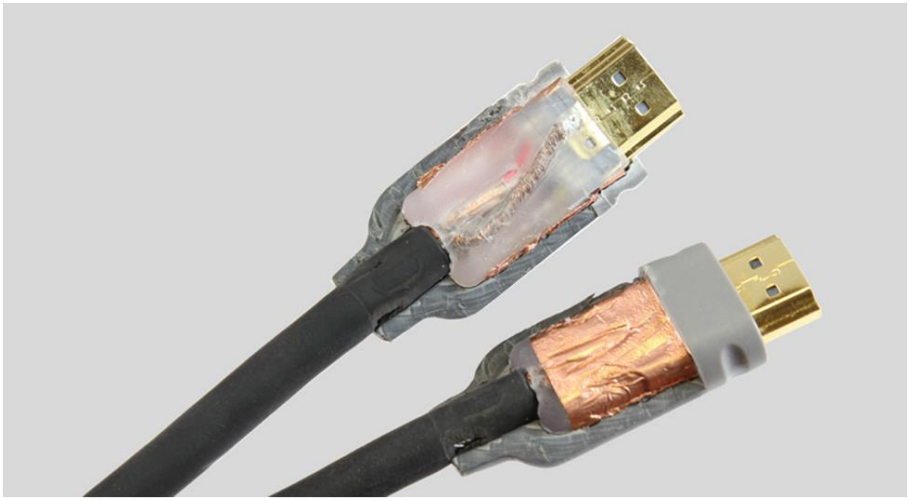

Figure 27 Left - Pigtail termination, Right - Foil termination

Figure 28 Left – Pigtail termination, Right – Foil termination

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Internal Cables

Internal cables are a critical path for emissions propagation from one area of the chassis to another. Care has to be taken with regard to internal cable routings especially with respect to flat ribbon cables. There is a misconception among designers that emissions are restricted to signals of high frequency and therefore DC cables and control leads need not be isolated. This could not be further from the truth. Any ungrounded metal or conductor is a potential path for emissions and should be treated so. Internal cable routings should be carried out with careful placement of the cables away from the PCB board - especially the high frequency are of the board where the oscillators and processors are situated. All cables should be secured with tie-downs to prevent loose cables falling onto or near the PCBs.

If ribbon cables are used, employing distributed ground return paths will help to keep the current loop areas to a minimum. Keep these cables as short as possible using the shortest route away from the PCB and I/O connectors.

Improper shield terminations are a common source of emissions on connectors. Where the shield does not make contact with the metal shell and the vinyl jacket then serves to create a small gap for emissions leak.

If a plastic shell is used for the connector housing, then the shield may be connected to ground by a pigtail onto the chassis ground as near to the connector as possible to keep the pigtail length to a minimum. While this is not an optimal termination, the pigtail can help to reduce emissions significantly if connected to the right point on the chassis. Grounding of the pigtail to signal ground is not a correct approach since the ground path to chassis ground is through the systems power supply.

Emissions from poorly shielded cables can further be reduced by application of filtering capacitors on each of the inner conductors to ground. The filter capacitors must be placed as close to the connector to be effective while keeping the capacitor leads as short as possible. Filter capacitors are typically between 100pf and 5600pf values depending on the type of signal present on the line being filtered. Too much capacitance may distort the signal significantly as to effect the functionality of the interface especially if long cable lengths are involved. Again if the capacitor value is limited by the distortion it may cause on the interface signal, in-line inductors may be added to enhance the filtering effect. As another option, ferrite mounts specifically designed for I/O connector mounts may be used to prevent high emissions from ever reaching the I/O cable.

The Ethernet Port

The proliferation of Ethernet connected devices means that the Ethernet port is now by far the most common interface port using unshielded twisted pair cables. If this port is not designed properly, severe emissions and immunity issues can arise. Data transfer rates of up to 1000 Mb/s are now common features and it is imperative to get the Ethernet magnetic connected and laid out correctly to minimize common mode emissions coupling onto the cables. The most common form of the Ethernet port is the un-powered variety. A typical RJ45 port can have integrated or discrete magnetics. In either case, the magnetics consist of a differential mode portion for balance and impedance matching of the Ethernet signal pair, and a common mode portion for rf choking the common mode emissions off each pair. It is important to understand just how easily the Ethernet port can be compromised even with the specially designed magnetics installed.

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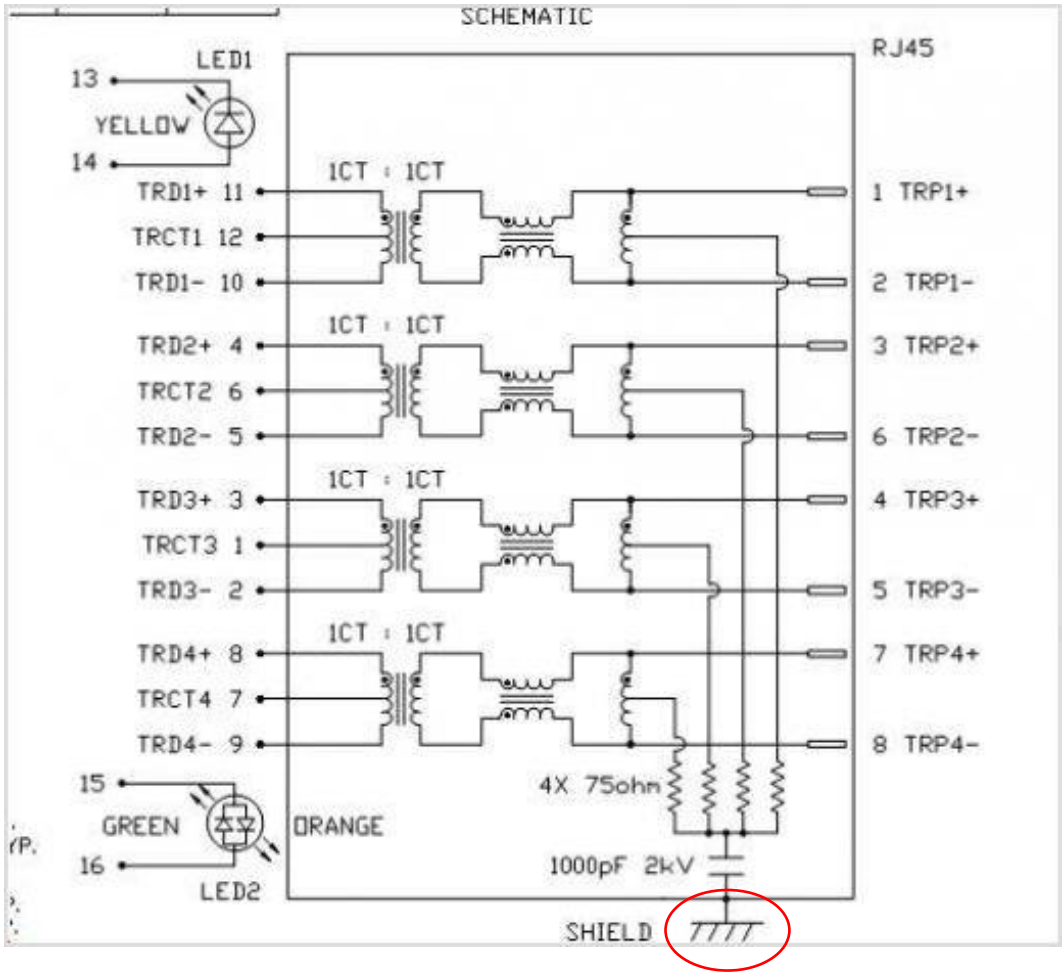

Figure 29 Ethernet RJ45 connector with integrated magnetics

Figure 29. depicts a typical RJ45 connector with built-in integrated magnetic and LED status leads. These connectors are usually shielded with the shield connected to mounting posts. All application notes on Ethernet connectors recommend connecting the centre tap 75ohm resistors to shield which is connected to the earth/chassis ground of the device.

On no account should this centre tap reference pin ever be connected to signal ground or any other ground other than chassis/shield. Doing so will provide a path for common mode noise on the signal ground plane to couple behind the Ethernet magnetic and directly radiate off the Ethernet connectors. In addition, due to reciprocity between EMI and EMC, the connection of this common-mode point to signal ground will allow external coupled noise coupled to the Ethernet cable, a bypass path around the Ethernet magnetics, into the signal ground plane of the device. If there is no earth/chassis ground due to the non-metallic housing of the device, it is more desirable to leave this common-mode reference point connected to the connector shell and floating rather than to attach it to any non-shield/chassis connection points.

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THE CHASSIS ENCLOSURE

The chassis enclosure is preferably metal or metal-coated plastic. If a cover or front panel is used, one has to ensure good electrical bonding along the seam edges. One aspect of a metal chassis housing is that they usually get painted or anodized which prevents the covers from making a good electrical bond with each other. This usually leads to slot antennas being formed along the cover edges and usually results in high frequency problems above 300MHz. The amount of leakage from a seam depends on the following:

1. The maximum linear dimension (not area) of the opening.
2. The wave impedance.
3. The frequency of the source.

The maximum radiation from a slot is when the length is equal to or less than a half-wavelength. The shielding effectiveness of a slot is equal to:

$$S = 20\log\left(\frac{\lambda}{2l}\right)$$

where: λ is the wavelength
l is the maximum dimension of the slot in inches

Reducing the slot by a half increases the shielding effectiveness by 6dB. It is suggested that to keep emissions from seams and vents to a minimum, the opening should be no greater than 1/20th the wavelength which will provide a shielding effectiveness of 20dB. The maximum slot length equivalents to 20dB at various frequencies are as follows:

Frequency (MHz)	Maximum Slot Length (Inches)
30	18
100	6
300	2
500	1.2
1000	0.6

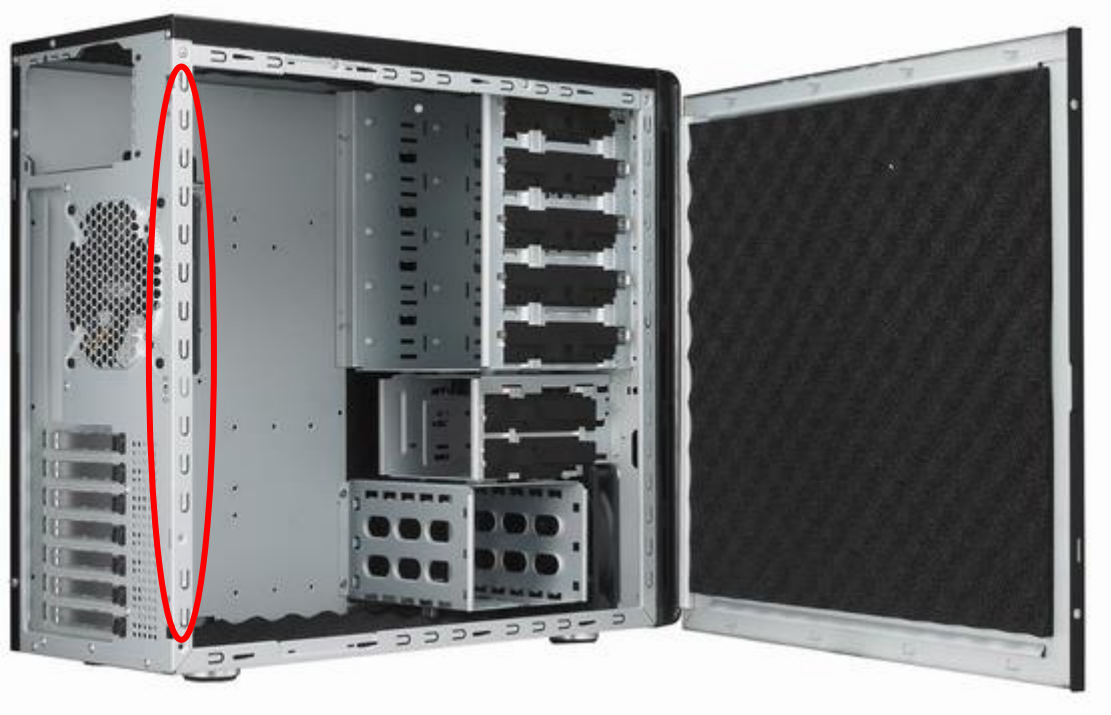

Figure 30 Case showing dimple punch outs along case seams to break up slot lengths

GROUNDING

Probably one of the most important aspects of EMC that is the least understood. Most refer to ground in terms of safety or earth ground and we have come to rely on the DC continuity test to check for continuity with a point to ground. In EMC terms, the DC continuity proves nothing as at high rf frequencies, strange things happen to the current such as it tends to travel more closely to the surface of a conductor the higher the frequency goes. This phenomenon is called skin effect and occurs largely in round conductors like the ground wires used in most electrical and electronic equipment today. Because the currents travel on the surface at high rf frequencies, there are fewer conductors being used and consequently an increase in resistance results in the conductor.

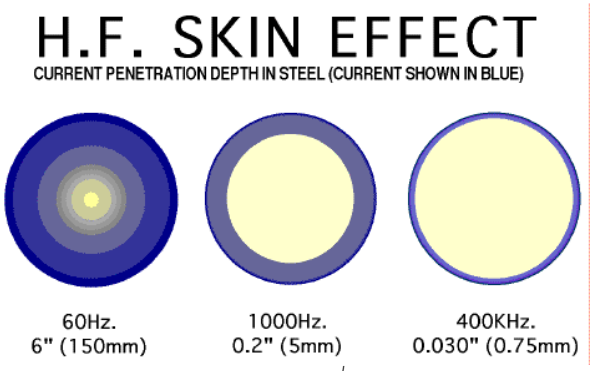

Figure 31 $R = 21 \sqrt{f} / r$ nΩ/m

For RF grounds to be formed, flat conductors such as braid or copper tape have significantly lower inductances than round wires and are therefore better suited to interconnect various metal structures within a system. The MIL-STD-461 defines a good high frequency ground strap as having a length to width ration of 5:1 and are commonly wide flat straps conductors used for bonding.

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Figure 32 Braided ground straps

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PREPARING A SAMPLE FOR EMC TESTS

- Cables should be properly terminated and securely mated. Shielded cables with metallic connector housings are highly recommended. All cable connectors should be screwed down to ensure proper shield to chassis ground contact. Improperly shielded cables are a primary source for non-compliance if the shield is not making a good electrical contact with chassis ground, failure is almost guaranteed. Just because a cable looks shielded doesn't mean it is. Open the connector housing and investigate how the shield has been terminated. In addition, investigate that the mating connector is directly grounded to the chassis housing.

- The EUT chassis should have proven ground continuity on all metal components. Star washers are a common way to ensure that painted metallic covers make good electrical contact with the rest of the chassis. Any metal covers that are not properly grounded will act as a sheet antennas radiating energy to the system cables and the surrounding peripherals.

- All opening and slots should be covered with metal panels or metal mesh, which make electrical contact with the chassis housing every few centimeters wherever possible. Shielding of Air vents used for internal cooling or aesthetic purposes may be carried out using grounded fine wire mesh to reduce the risk of a slot antenna effect from the vents slots. Ventilation slots should be implemented with holes rather than slots.

- Filters used on power lines or I/O connectors should be mounted as close to the cable entry point to be effective. Some systems extend the power cord to the front of the chassis for user accessibility to the power switch. In this case the ac power line filter should be placed on the ac cord at the point where it enters the chassis.

- Crystals and high frequency oscillators mounted too close to the I/O connectors or any openings in the chassis make obtaining compliance that much more difficult. Placement of high frequency oscillators should be done with the following in mind;

    1. Keeping the trace leads that carry the high frequency components as short as possible. In multiplayer designs, these traces should be sandwiched between the ground and power planes with guard traces run along either side of the trace in the same plane.

    2. For long high frequency carrying trace leads, Pico-farad coupling capacitors or ferrite beads may be used to bleed off some of the higher frequency components. Matching resistors at the source end of the trace also should be provided.

    3. High frequency components may be isolated from the rest of the chassis by placing them in a separate metallic grounded enclosure or by using picket fences.

- Internal cabling and routing can have a significant effect on obtaining compliance. Cable routes should be selected to be as far from high frequency components as possible and as close to the chassis housing as possible. Chassis eyelets along cable routes assist in securing the internal cables to selected routes to minimize repeatability issues during the tests. Flat ribbon cables are a common form of interconnecting sub-assemblies. Due to the nature of the ribbon cable, they are very good radiators and susceptors of emission energy and so extra care in ribbon cable routings should be taken. Using shielded cables or

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metallic ducts for internal cable interconnects significantly adds to the design margin for obtaining compliance provided the shields could be properly terminated.

- For plastic and non-metallic enclosures that contain unshielded high frequency components, metallic coatings such as nickel or copper can be applied to the inside of the units to provide the shielding necessary to obtain compliance. Aluminum vacuum coating has been shown to provide consistent and uniform coverage.

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FINDING A COST-EFFECTIVE SOLUTION TO NON-COMPLIANCE

PCB Layout

Any modification to a finished system will add significant costs to the final production unit. It is therefore important to reduce the emissions at a very early stage in a products development cycle since board level fixes during the early stages of development are the most cost-effective solutions to emission problems. Designing for EMI compliance is normally carried during the PCB layout stage where location of the high frequency components and trace layouts are determined. Some design engineers will leave plated through holes or surface mounting pads at strategic places on the PCB, to allow for the addition of filter capacitors or in-line ferrites/inductors on the prototype boards.

The prototype PCB may then be probed for hot spots using a high frequency oscilloscope or spectrum analyzer. What design engineers look for is high-speed waveforms with a rich harmonic content. Once the hot spots have been localized, appropriate suppression filters may be added to reduce high harmonic content on the trace while preserving the signal integrity. These is sometimes referred to as the cut and try method whereby various positions on a trace are cut and RF chokes added to determine the most effective location for the filter.

Cable, Cables, Cables....

Unshielded cables and flat ribbon cables are a primary concern to any EMI engineer because of their potential for becoming wire antennas if the emissions are not properly contained in the EUT chassis. Cables and their associated connectors are usually the first area checked if emissions are found to exceed the limits. Typically, cables will be disconnected one at a time in an attempt to isolate where the emissions are emanating from Once the source has been detected various options are available in reducing the emissions radiating from a cable.

- Using a shielded cable
- Placing filtering capacitors and ferrites on the I/O connector if the connector is PCB mounted.
- Placing a ferrite choke on the cable right at the connector. The number of turns through the choke determines the attenuation of the emissions.

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Chassis Construction

Construction of the chassis is considered when it has been determined that the emissions are not coming from the I/O connectors/cables. Checks are made on the following;

- The mating of the enclosure cover with the chassis frame is checked for gaps and slots where emissions could possibly leak.
- Electrical continuity between the cover and chassis is checked to ensure that good electrical bonding is occurring.
- Emissions from vents or slots are checked by temporarily covering them with copper tape to see if this reduces the level of emissions. If this is the case, modifications with fine wire mesh may be used to prevent emissions leak from the EUT.
- Some front covers on EUT are non-metallic resulting in high emissions being measured from the front of the EUT. Conductive coatings such as nickel or copper based may be applied with special attention given to how the cover will be electrically bonded with the chassis frame. The preferred approach is to have the electrical bonding all around the edge of the cover panel so that it provides a good emission seal to the front panel.

Any modifications for compliance are a costly consequence. It is more easily achieved and much more cost-effective when conducted at the design stages than to carry out the modifications in the production phase. For companies that do not design with EMI compliance in mind, the risk of failing a qualification test is about 80%. The associated cost and time of getting a non-compliant product to market should be weighed off against the cost of implementing some EMI compliance programs within the organization. Education of product and design engineers into the additional requirements of not only designing for functionality but also for compliance should be carried out at a minimum.

Product and design engineers are urged to witness EMI compliance tests to familiarize them with the potential problem areas associated with their product line. It is quite often that fixes made on a single model can be carried over to other models of a production line with great success. In this way, design and product engineers will improve the compliance of their products by incorporating previous suppression techniques at the board level into later models.

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EMC DESIGN GUIDE SUMMARY

Chassis:	A completely enclosed metal chassis is the preferable enclosure. Care should be taken to ensure that along the scam edges, good electrical bonding is made between any covers and chassis. This usually means paint masking at overlapping joint areas, use of beryllium-copper fingers or conductive polymer gaskets. If a plastic enclosure is necessary due to marketing pressures, it is recommended that a tin enclosure inside the plastic chassis still be used to house the high frequency PCBs much the same way TV and radio circuits are isolated. Failing this, metallized coating will be a minimal requirement in the presence of PCBs with high density, high speed logic.
PCBs:	Multilayer PCBs with ground and supply planes are generally about 10dB quieter than equivalent double sided PCBs. More suppression can be obtained by burying the high frequency traces between, ground and supply planes. The catch with burying too many traces inside the PCB is that it makes trouble-shooting the board extremely difficult. Ensure that there are no copper planes underneath I/O connectors and their filter circuits except chassis ground plane. On the PCB edges, back off all signal traces from the edge by a couple of millimeters.
Trace lengths:	All high frequency components should be localized near the centre of the PCB away from jumper, I/O connectors, internal cable routes and main BUS areas. All high frequency traces should be kept as short as possible so that IC placement should be dictated by the optimal length of hot traces around the PCB.
Pads for suppression:	When laying out a PCB, it never hurts to design in suppression components for de-coupling capacitors and maybe even in-line ferrites and terminating resistors used in reducing ringing in clock traces. This especially useful with regard to RS-232, parallel port interfaces and telecommunications interfaces. The PCB need not be populated until the suppression components are proved necessary and if this occurs, no re-layout of the PCB needs be carried out to achieve compliance.
I/O connectors:	Shielded cables are recommended where possible. The shield should be terminated with a 360 degree contact onto the I/O connector shell. The shield should always be ground directly to chassis and not to signal ground.
Pigtails:	Avoid at all cost. Keep it as short as possible if you have to use it. Pigtails cause us no end of trouble – even the 1” variety.
SST Clock:	Spread spectrum clock should be used wherever possible.

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Internal cable routes: Route cable as far away from high frequency oscillators and components. Also ensure that they are neatly bundled and tied down. If flat ribbon cable is used, make it as short as possible and select the mounting headers on the PCB board away from high frequency components and traces.

Grounding: I am convinced that there is no right: way to ground a PCB with regard to EMC. In general, most PCB designs come with four or five grounding points which directly tie the signal ground to chassis across the PCB. We have observed limited success in reducing emissions by removing some of these ground points from certain motherboards – especially in the areas of the high frequency oscillators. Our approach is still trial-and error and we go with whatever works.

With respect to ESD, proper grounding of all metal throughout a product must be made. A resistance of a few ohms is insufficient electrical bonding to prevent large amount of potential difference in the sub-nano second events of a discharge. Ensuring-that all metal components jump at the same time is one key to meeting ESD threats.

Grounding braids which are flat and wide should be used over round wires to interconnect internal metal frames.

Separate ground grids should be maintained for analogue, digital, hardware and chassis grounds with one common point at the power supply secondary. It is also a good idea to keep the various circuits isolated from each other on the PCB.

Shielded cable in a desktop environment should be grounded to chassis ground at both ends. In distributed systems, care should taken with the shield since large potential differences in the earth grounds at different location s will introduce large current loops which are carried on the cable shield. In certain cases, a hybrid ground may be used by connecting the shield to ground at one location through a 0.1uf capacitor.

Air vents: Air vents of the multiple hole variety are preferable. Vent slots may used so long as the slot length is kept to less than $1/10^{th}$ of the highest frequency wavelength encountered in the product. Since the highest frequency component is usually a harmonic of one of the internal oscillators, the optimal slot length may no easily be determined.

Power Supplies: Power supply filters and surge suppressors should be lace as close to the point of entry as possible. Any exposed length of power supply line routed internally should be shielded of isolated from the PCB. The most effective power supply filters are shoes incorporated in the AC receptacle plug. Remember, the ac line filter is to protect the hydro network from receiving RF noise from your device – not that other way around.

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In switches, care should be taken on routing internal cables away from switching transistors and the high voltage transformers as harmonics of these are often observed in VDE and CISPR conducted emissions measurements which begin at 10 KHz and 150 KHz respectively. All main switching diodes and FETS must have the ringing reduced using snubber networks usually of the order of 100pf/1000ohms. This is also true of the feedback control signal which also may have to be treated with ferrites to reduce high frequency content.

Overloading or under loading a switching power supply causes more switching noise to be generated - especially if an external switcher is used as in the case of laptops.

Minimizing crystals: As the number of crystal oscillators increase, so do your chances of running into a emissions problem. Although this is a broad generalization, we've had a lot more success with single oscillator products where all timing is derived off one clock. Personal computer motherboards are trending towards this with single frequency synthesizer chips for the main processor and video function.